

What is claimed is:

1 1. An input circuit comprising:
2 a data input means for the input of input data;
3 a data latch means for latching the input data;
4 a reset means for resetting the data latch means;
5 a clock synchronization means for synchronizing the input
6 of the input data to the data input means; and
7 a latch enhancement means for blocking feedthrough current
8 by functioning complementarily to the reset means, and enhancing
9 the latching operation of the data latch means.

1 2. An input circuit comprising:
2 a data input means for the input of input data;
3 a data latch means for latching the input data;
4 a reset means for resetting the data latch means;
5 a clock synchronization means for blocking feedthrough
6 current by functioning complementarily to the reset means and
7 synchronizing the input of the input data to the data input means;
8 and
9 a latch enhancement means for enhancing the latching
10 operation of the data latch means.

1 3. An input circuit comprising:
2 a data input means for the input of input data;
3 a data latch means that provides a combined function of
4 blocking feedthrough current in the reset state and synchronizing
5 the latch of the input data;

6 a reset means for resetting the data latch means; and
7 a latch enhancement means for enhancing the latching
8 operation of the data latch means.

1 4. The input circuit of claim 1, wherein the data latch
2 means has a configuration in which the sources of a first PMOS
3 transistor and a second PMOS transistor are connected to a first
4 power source; the drains of the first PMOS transistor and a first
5 NMOS transistor, and the gates of the second PMOS transistor
6 and a second NMOS transistor are connected to a second output
7 terminal; the drains of the second PMOS transistor and the second
8 NMOS transistor and the gates of the first PMOS transistor and
9 the first NMOS transistor are connected to a first output
10 terminal; the source of the first NMOS transistor is connected
11 to a first common terminal at which one of a pair of complementary
12 signals constituting the input data appears; and the source of
13 the second NMOS transistor is connected to a second common
14 terminal at which the other one of the pair of complementary
15 signals constituting the input data appears.

1 5. The input circuit of claim 1, wherein the reset means
2 includes the sources of a third PMOS transistor and a fourth
3 PMOS transistor being connected to the first power source; the
4 drain of the third PMOS transistor being connected to the first
5 output terminal; the drain of the fourth PMOS transistor being
6 connected to the second output terminal; and the gates of the
7 third PMOS transistor and the fourth PMOS transistor being

8 connected to a first clock input terminal.

1 6. The input circuit of claim 1, wherein the data input
2 means includes a third NMOS transistor being connected to a first
3 data input terminal; the gate of a fourth NMOS transistor being
4 connected to a second data input terminal; the drain of the third
5 NMOS transistor being connected to the first common terminal;
6 the drain of the fourth NMOS transistor being connected to the
7 second common terminal; and the sources of the third NMOS
8 transistor and the fourth NMOS transistor being connected to
9 a third common terminal to which power is supplied from a second
10 power source.

1 7. The input circuit of claim 1, wherein the clock
2 synchronization means includes the gate of a fifth NMOS
3 transistor being connected to the first clock input terminal;
4 the drain of the fifth NMOS transistor being connected to the
5 third common terminal; and the source of the fifth NMOS transistor
6 being connected to the second power source.

1 8. The input circuit of claim 1, wherein the latch
2 enhancement means includes the gates of a sixth NMOS transistor
3 and a seventh NMOS transistor being connected to a second clock
4 input terminal; the sources of the sixth NMOS transistor and
5 the seventh NMOS transistor being connected to the second power
6 source; the drain of the sixth NMOS transistor being connected
7 to the output end of the current path of a first

8 feedthrough-current blocking means; the drain of the seventh
9 NMOS transistor being connected to the output end of the current
10 path of a second feedthrough-current blocking means; the input
11 end of the current path of the first feedthrough-current blocking
12 means being connected to the first common terminal; the input
13 end of the current path of the second feedthrough-current
14 blocking means being connected to the second common terminal;
15 and the control terminals of both the first and second
16 feedthrough-current blocking means being connected to the first
17 clock input terminal.

1 9. The input circuit of claim 1, wherein the first and
2 second feedthrough-current blocking means includes the gates
3 of both an eighth NMOS transistor and a ninth NMOS transistor
4 being connected to the first clock input terminal; the drain
5 of the eighth NMOS transistor being connected to the first common
6 terminal; the drain of the ninth NMOS transistor being connected
7 to the second common terminal; the source of the eighth NMOS
8 transistor being connected to the drain of the sixth NMOS
9 transistor; and the source of the ninth NMOS transistor being
10 connected to the drain of the seventh NMOS transistor.

1 10. The input circuit of claim 2, wherein the data input
2 means includes the sources of both a tenth NMOS transistor and
3 an eleventh NMOS transistor being connected to the second power
4 source; the gate of the tenth NMOS transistor being connected
5 to a first data input terminal; the gate of the eleventh NMOS

6 transistor being connected to a second data input terminal; the
7 drain of the tenth NMOS transistor being connected to a third
8 common terminal at which one of a pair of complementary signals
9 constituting the input data appears; the drain of the eleventh
10 NMOS transistor being connected to a fourth common terminal at
11 which the other one of the pair of complementary signals
12 constituting the input data appears.

1 11. The input circuit of claim 2, wherein the clock
2 synchronization means includes the gates of twelfth NMOS
3 transistor and thirteenth NMOS transistor being connected to
4 the first clock input terminal; the source of the twelfth NMOS
5 transistor being connected to a third common terminal at which
6 one of a pair of complementary signals constituting the input
7 data appears; the source of the thirteenth NMOS transistor being
8 connected to a fourth common terminal at which the other one
9 of the pair of complementary signals constituting the input data
10 appears; the drain of the twelfth NMOS transistor being connected
11 to a first common terminal; and the drain of the thirteenth NMOS
12 transistor being connected to a second common terminal.

1 12. The input circuit of claim 2, wherein the latch
2 enhancement means includes the sources of both a fourteenth NMOS
3 transistor and a fifteenth NMOS transistor being connected to
4 a second power source; the gates of both the fourteenth NMOS
5 transistor and the fifteenth NMOS transistor being connected
6 to a second clock input terminal; the drain of the fourteenth

7 NMOS transistor being connected to a third common terminal at
8 which one of a pair of complementary signals constituting the
9 input data appears; and the drain of the fifteenth NMOS transistor
10 being connected to a fourth common terminal at which the other
11 one of the pair of complementary signals constituting the input
12 data appears.

1 13. The input circuit of claim 3, wherein the data latch
2 means includes the sources of both a first PMOS transistor and
3 a second PMOS transistor being connected to a first power source;
4 the drain of the first PMOS transistor, the gates of the second
5 PMOS transistor and the nineteenth NMOS transistor, and the input
6 end of the current path of a first clock-synchronization
7 feedthrough-current blocking means being connected to a second
8 output terminal; the gate of the first PMOS transistor, the drain
9 of the second PMOS transistor, the gate of the eighteenth NMOS
10 transistor, and the input end of the current path of a second
11 clock-synchronization feedthrough-current blocking means being
12 connected to a first output terminal; the drain of the eighteenth
13 NMOS transistor being connected to the output end of the current
14 path of the first clock-synchronization feedthrough-current
15 blocking means; the drain of the nineteenth NMOS transistor being
16 connected to the output end of the current path of the second
17 clock-synchronization feedthrough-current blocking means; the
18 source of the eighteenth NMOS transistor being connected to a
19 third common terminal at which one of a pair of complementary
20 signals constituting input data appears; the source of the

21 nineteenth NMOS transistor being connected to a fourth common
22 terminal at which the other one of the pair of complementary
23 signals constituting input data appears; and the control terminal
24 of the first clock-synchronization feedthrough-current
25 blocking means being connected to the first clock input terminal.

1 14. The input circuit of claim 13, wherein the first
2 clock-synchronization feedthrough-current blocking means
3 includes the drain of a sixteenth NMOS transistor being connected
4 to a first input end; the gate of the sixteenth NMOS transistor
5 being connected to a third input end; and the source of the
6 sixteenth NMOS transistor being connected to a first output end;
7 and the second clock-synchronization feedthrough-current
8 blocking means includes the drain of a seventeenth NMOS
9 transistor being connected to a second input end; the gate of
10 the seventeenth NMOS transistor being connected to a fourth input
11 end; and the source of the seventeenth NMOS transistor being
12 connected to a second output end.